Please amend the subject application as follows:

IN THE CLAIMS:

Please cancel claims 2 and 31-59 without prejudice and accept amended claims 1, 3, 5, 8-13, 16-21, 24, 25, 27-30 and 60 and new claims 61-65 as follows:

1. (currently amended) A method of forming cooling elements in a semiconductor substrate, comprising:

coating a backside of the semiconductor substrate with a first mask layer;

forming a plurality of trench patterns in the first mask layer;

etching the semiconductor substrate to form a plurality of trenches along the plurality of trench patterns; [[and]]

depositing thermally conductive material in the plurality of trenches;

forming a first diffusion layer in the semiconductor substrate;

forming a second diffusion layer in the first diffusion layer; and

doping the second diffusion layer with a dopant having a polarity opposite a polarity of the semiconductor substrate.

2. (canceled)

3. (currently amended) The method as recited in claim [[2]] 1, further comprising stopping the etching of the semiconductor substrate ~~when the dopant contained in~~ at the second diffusion layer ~~is detected in a product of the etching~~.

4. (original) The method as recited in claim 1, wherein the first mask layer is a photoresist.

5. (currently amended) The method as recited in claim 1, wherein the trench patterns are formed by [[one of]] optical, x-ray, extreme ultra-violet, electron beam [[and]] or ion beam lithographic techniques.

6. (original) The method as recited in claim 1, wherein etching of the semiconductor substrate is performed with Cl_2-based plasma.

7. (original) The method as recited in claim 1, wherein the plurality of trenches are formed in the vertical direction.

8. (currently amended) The method as recited in claim 1, wherein the step of depositing thermally conductive material is performed by [[one of]] chemical vapor deposition, atomic layer deposition, physical vapor deposition [[and]] or electroplating.

9. (currently amended) The method as recited in claim 1, wherein the thermally conductive material is made from [[one of]] aluminum nitride, aluminum, copper-tungsten, silicon carbide, gold, copper, diamond [[and]] or silver.

10. (currently amended) The method as recited in claim 1, wherein the semiconductor substrate is [[one of]] a complimentary metal oxide semiconductor wafer [[and]] or a silicon-on-insulator wafer.

11. (currently amended) The method as recited in claim 1, wherein the plurality of trenches are formed in an ~~intergrated~~ integrated-circuit chip of the semiconductor substrate.

12. (currently amended) The method as recited in claim 1, wherein the step of etching the semiconductor substrate to form the plurality of trenches is performed away from at least [[one of]] a passivation layer, an interconnect layer, a device layer [[and]] or a doped well structure of the semiconductor substrate.

13. (currently amended) The method as recited in claim 1, wherein the plurality of trenches are formed [[one of]] before [[and]] or after processing of remaining portions of the semiconductor substrate.

14. (original) The method as recited in claim 1, further comprising integrating an external heat sink on the backside of the semiconductor substrate.

15. (original) The method as recited in claim 1, further comprising integrating an active cooling apparatus on the backside of the semiconductor substrate.

16. (currently amended) The method as recited in claim 15, wherein the step of integrating the active cooling apparatus on the backside of the semiconductor substrate includes:

coating the backside of the semiconductor substrate with a second mask layer;

patterning the second mask layer;

etching a continuous trench into the backside of the semiconductor substrate;

forming at least one opening in the continuous trench for allowing coolant supplied from the active cooling apparatus to [[one of]] exit [[and]] or enter the continuous trench; and

positioning the active cooling apparatus on the backside of the semiconductor substrate.

17. (currently amended) The method as recited in claim 15, wherein the active cooling apparatus is [[one of]] a thermal electric cooling component, a micro-fan device [[and]] or a micropump.

18. (currently amended) The method as recited in claim 15, wherein the active cooling apparatus is [[one of]] directly fabricated on the backside of the semiconductor substrate [[and]] or separately built and mounted on the backside of the semiconductor substrate.

19. (currently amended) A method of forming an active cooling apparatus on a

semiconductor substrate, comprising:

coating the backside of a first semiconductor substrate with a mask layer;

patterning the mask layer;

etching a first continuous trench into the backside of the first semiconductor substrate;

forming at least one opening in the first continuous trench for allowing coolant supplied from the active cooling apparatus to [[one of]] exit [[and]] or enter the first continuous trench; and

positioning the active cooling apparatus on the backside of the first semiconductor substrate.

20. (currently amended) The method as recited in claim 19, wherein the active cooling apparatus is [[one of]] a thermal electric cooling component, a micro-fan device [[and]] or a micropump.

21. (currently amended) The method as recited in claim 19, wherein the active cooling apparatus is [[one of]] directly fabricated on the backside of the first semiconductor substrate [[and]] or separately built and mounted on the backside of the first semiconductor substrate.

22. (original) The method as recited in claim 19, further comprising:

forming a second semiconductor substrate including a second continuous trench; and

fastening the second semiconductor substrate to the first semiconductor substrate at a position between the backside of the first semiconductor substrate and the active cooling apparatus, whereby the active cooling apparatus rests on the second semiconductor substrate.

23. (original) The method as recited in claim 22, wherein the second continuous trench is a mirror image of the first continuous trench of the first substrate.

24. (currently amended) The method as recited in claim 22, wherein the step of fastening includes [[one of]] anodic bonding [[and]] or metallurgical soldering.

25. (currently amended) The method as recited in claim 22, wherein the second semiconductor substrate includes at least one opening in the second continuous trench for allowing the coolant supplied from the active cooling apparatus to [[one of]] exit [[and]] or enter the second continuous trench.

26. (original) The method as recited in claim 19, wherein the mask layer is a photoresist.

27. (currently amended) The method as recited in claim 19, wherein the first continuous trench is formed to be larger in the horizontal direction than in the vertical direction.

28. (currently amended) The method as recited in claim 19, wherein the first semiconductor substrate is [[one of]] a complimentary metal oxide semiconductor wafer [[and]] or a silicon-on-insulator wafer.

29. (currently amended) The method as recited in claim 22, wherein the second semiconductor substrate is [[one of]] a silicon substrate [[and]] or a plate-glass substrate.

30. (currently amended) The method as recited in claim 19, wherein the first continuous trench is formed in an ~~intergrated~~ integrated-circuit chip of the first semiconductor substrate.

31. - 59. (canceled)

60. (currently amended) A method of forming cooling elements in a semiconductor substrate, comprising:

etching the semiconductor substrate from a backside of the semiconductor substrate to form a plurality of trenches; [[and]]

depositing thermally conductive material in the plurality of trenches;

forming a diffusion layer in the semiconductor substrate; and

doping the diffusion layer with a dopant having a polarity opposite a polarity of the semiconductor substrate.

61. (new) A method of forming an active cooling apparatus on a semiconductor substrate, comprising:

coating the backside of a semiconductor substrate with a mask layer;

patterning the mask layer;

etching a continuous trench into the backside of the semiconductor substrate;

forming two openings in the continuous trench for respectively allowing coolant supplied from the active cooling apparatus to exit and enter the continuous trench; and

positioning the active cooling apparatus on the backside of the semiconductor substrate.

62. (new) The method as recited in claim 61, wherein the coolant is gas or liquid.

63. (new) The method as recited in claim 61, wherein the coolant flows through the continuous trench.in a horizontal direction.

64. (new) The method as recited in claim 61, wherein the continuous trench.includes a plurality of channels.

65. (new) A method of forming an active cooling apparatus on a semiconductor substrate, comprising:

etching a continuous trench having a plurality of channels into the backside of the semiconductor substrate;

forming an opening in the continuous trench, wherein coolant supplied from the active cooling apparatus passes through the opening; and

positioning the active cooling apparatus on the backside of the semiconductor substrate.